Power Supply Noise Coupling between Different Power Domains in a Large Programmable SoC

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Motivation

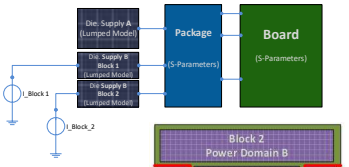
- **Programmable SoCs are used in a variety of applications**
  - AI, Cloud Services, IoT, Machine Vision, Network Acceleration, etc.
  - There is increasing demand for large integrated systems that combine multiple IPs in one chip
- **Large number of different blocks have to coexist and interact within SoC**
  - Every block has its own power demands, restrictions, and requirements
  - Power Integrity needs to be maintained across the system: die, package, and board
  - Some systems are large and distributed by nature. Power delivery networks of such systems can have a lot of shared return path
  - While it is possible to isolate the power routing and planes, the return path is usually common
  - There are scenarios when a large transient event in one power domain can cause a significant amount of noise to couple to another supply through shared ground
  - Distributed nature of the problem requires the use of appropriate methodology and tools for PI analysis
  - For the first order power supply noise evaluation within a single power domain it is possible to use simplified (even lumped) models for on-die power distribution network (PDN). For cross-domain noise coupling study a model has to capture the distributed nature of the PDN. We collaborated with ANSYS to adopt ANSYS Chip Power Model (CPM) for die-level PDN modeling

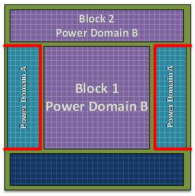
Main Idea

- We study a system built around a large Xilinx programmable SoC device
- We consider two power supplies (A and B) distributed across the chip and sharing the return path
- Circuitry in power domain A (aggressor) can quickly start/stop switching creating a large current spike
- Coupling across power domains can potentially cause significant voltage noise in supply B
- We need to verify that noise on the victim supply B stays within acceptable limits
- The coupling has to be studied on a system level
  - Die (Lumped or distributed circuit model)
  - Package (S-parameter model)
  - Board (S-parameter model)
- Distributed models required to capture the coupling
- We consider two cases
  - 1. A and B are well isolated on die (both power and ground are separated) and only share ground in package and board
  - 2. A and B have shared return path in top metal layers of the silicon as well as in package and board

Model Setup. Assuming Perfect On-Die Isolation

- Assumptions:
  - **Die**
    - Good isolation between the supplies
    - **Simple lumped models** for on-die PDN
  - **Package**
    - Layout-based S-parameters
    - Two versions of the model:
      - Combined ground
      - Slotted ground
  - **Board**
    - Layout-based S-parameters

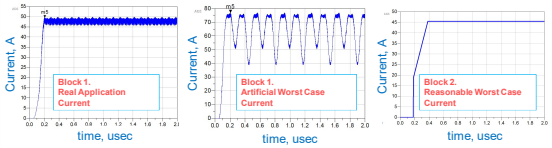




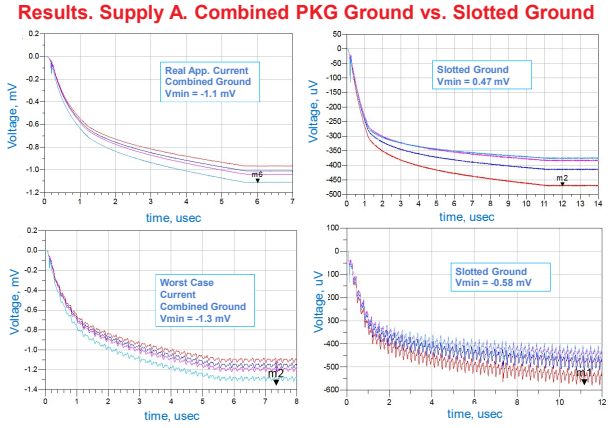
Additional measure to reduce coupling:
Ground planes in the package are slotted above the core layer

Transient Current Profiles

- Two current profiles for Block 1 in Supply B:
  - The real high-power application: ~50A dynamic current
  - Artificial (synchronized) worst case: > 65A dynamic current
- Realistic worst case for Block 2 in Supply B:
  - 18A in 2ns, then up to 45 A in the next 200ns



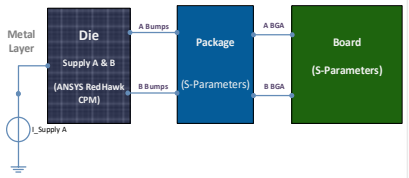
Results. Supply A. Combined PKG Ground vs. Slotted Ground

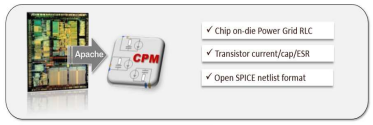


	Real App Case		Worst Case	
	Combined GND	Slotted GND	Combined GND	Slotted GND
Noise on Supply A, mV	1.1	0.47	1.4	0.58

Model Setup. Assuming On-Die Coupling Cannot Be Ignored

- Setup:
  - Die
    - **RedHawk CPM** from layout
    - Ports on Metal 7 and on PKG bump level
    - Grounds are merged on the top layer
  - Package
    - S-parameters
    - 2.5D extraction from layout
  - Board
    - S-parameters
    - 2.5D extraction from layout

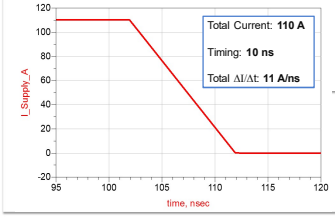




- Multi-domain, distributed model
- DC to multi-GHz validity
- Advanced chip excitation modes
- Silicon correlated

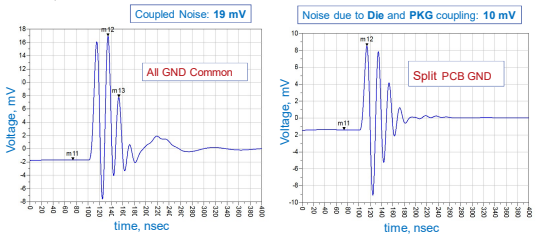
Transient Current Profile

- Supply A power down event
  - Modeled with a pwl current source



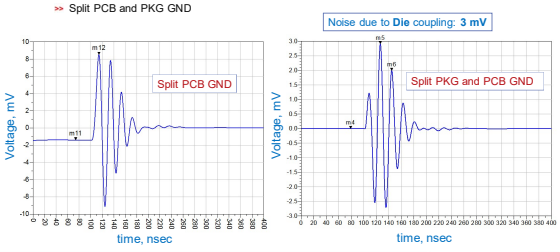
Noise on Supply B at C4 Bump. Die and PKG Contribution

- Setup:
  - All Ground Combined
  - Split Ground on PCB



Noise on Supply B at C4 Bump. Die-Level Coupling Only

- Setup:
  - Split PCB GND
  - Split PCB and PKG GND



Summary

- We performed a system-level analysis of power supply coupling between different domains in a system built around a large programmable Xilinx SoC chip
- ANSYS Chip Power Model (CPM) was used to extract a distributed model of the silicon-level PDN. The model allowed us to capture coupling between the two power supplies at the die level
- The results demonstrate that significant coupling exists. However, the system is robust enough, so that dumping 110 A of current within 10 ns only produces 19 mV of coupled noise
- Further study was done to conclude that the coupling happens through the shared return path (aka 'ground bounce')
- Additional experiments were performed to separate contributions of different system components (die, package, board) to the overall noise level

	Die	Package	Board	Total
Coupled Noise on Supply B, mV	3	7	9	19

References

1. Dmitry Klokotov, Jin Shi, Yong Wang, "Distributed Modeling and Characterization of On-Chip/System Level PDN and Jitter Impact," DesignCon 2014
2. Larry Smith, Shishuang Sun, Peter Boyle, "On-Chip PDN Noise Characterization and Modeling," DesignCon 2010